GPU Algorithm Design

Parallel primitives – Scan operation
Scan primitive

**Definition:**

\[
\text{Scan}(\oplus, \varepsilon, [a_0, a_1, a_2, \ldots, a_{n-1}]) = [\varepsilon, \varepsilon \oplus a_0, \varepsilon \oplus a_0 \oplus a_1, \varepsilon \oplus a_0 \oplus a_1 \oplus a_2, \ldots, \\
\varepsilon \oplus a_0 \oplus \cdots \oplus a_{n-2}]
\]

**Example:**

\[
\text{Scan}(+, 0, [3 1 7 0 4 1 6 3]) = [0 3 4 11 11 15 16 22]
\]

**Specification:**

The defined Scan is an *exclusive* scan

An *inclusive* Scan returns \([a_0, a_0 \oplus a_1, a_0 \oplus a_1 \oplus a_2, \ldots, a_0 \oplus \cdots \oplus a_{n-1}]\)

**Implementation:**

Coming next - for \(\text{Scan}(+, 0, \ldots)\), also called Prefix-Sum.
Sequential implementation

```c
void scan(int* in, int* out, int n)
{
    out[0] = 0;
    for (int i = 1; i < n; i++)
    
        out[i] = in[i-1] + out[i-1];
}
```

**Complexity:** $O(n)$
Parallel implementation - naïve

for (d = 1; d < \log_2(n); d++)
    for 0 ≤ k < n in parallel
        if( k ≥ 2^{d-1} )
            x[out][k] = x[in][k - 2^{d-1}] + x[in][k]
        else
            x[out][k] = x[in][k]
    swap(in, out)

“Complexity”: \(O(n \log_2 n)\)

Q: Why Double-Buffer?
Parallel implementation

- The naïve implementation is less efficient than the sequential.
- We want $O(n)$ operations in total.

Solution (Blelloch’90):
- Balanced trees. Build a balanced binary tree on the input data and sweep it to and from the root to compute the prefix sum.
- Complexity: $O(n)$.

- The algorithm consists of two phases:
  - Reduce (also known as the up-sweep)
  - Down-sweep
Up-Sweep

Traverse the tree from leaves to root computing partial sums at internal nodes of the tree.

```
for d := 0 to log₂n - 1 do
    for k from 0 to n - 1 by 2^(d+1) in parallel do
        x[k + 2^(d+1) - 1] := x[k + 2^d - 1] + x[k + 2^(d+1) - 1]
```

Sum of all elements. What collective operation that we know returns this value?
Down-Sweep

**Traverse back up the tree from the root, using the partial sums.**

\[
x[n - 1] := 0
\]

for \( d := \log_2 n \) down to 0 do

for \( k \) from 0 to \( n - 1 \) by \( 2^{d+1} \) in parallel do

- \( t := x[k + 2^d - 1] \)
- \( x[k + 2^d - 1] := x[k + 2^{d+1} - 1] \)
- \( x[k + 2^{d+1} - 1] := t + x[k + 2^{d+1} - 1] \)

Replace last element with 0. Do we need that value?
GPU Architecture (simplified)
Execution model

CUDA kernel

Blocks independently scheduled on MPs

Thread block

Run on a single MP
Threads coordinate

Warp

Threads run in lock-step
Implementation detail

Thread

Runs on a CUDA core
Execution model details

- SIMD Execution of threads in a *warp* (currently 32 threads).
- A group of warps executing a common task is a *thread-block*. The size of a thread-block is limited (e.g. to 1024 threads).
- Threads in the same thread-block are:
  - Executed on the same Multi-Processor (GPU core)
  - Enumerated – locally (in thread-block) and globally
  - Share data and synchronize
- Threads in different thread-blocks cannot cooperate
- Number of thread-blocks is (practically) unlimited.
CUDA Implementation (1/2)

```
__global__ void prescan(float *g_odata, float *g_idata, int n)
{
    extern __shared__ float temp[];  // points to shared memory
    int thid = threadIdx.x;
    int offset = 1;
    temp[2*thid] = g_idata[2*thid];  // load input into shared memory
    temp[2*thid+1] = g_idata[2*thid+1];
    for (int d = n/2; d > 0; d /= 2)  // build sum in place up the tree
    {
        __syncthreads();
        if (thid < d)
        {
            int ai = offset*(2*thid+1)-1;
            int bi = offset*(2*thid+2)-1;
            temp[bi] += temp[ai];
        }
        offset *= 2;
    }
    // continues on next slide
```

for $d := 0 \text{ to } \log_2 n - 1 \text{ do}$
for $k$ from $0 \text{ to } n - 1$ by $2^d + 1$ in parallel do

\[ x[k + 2^d - 1] := x[k + 2^d - 1] + x[k + 2^d + 1 - 1] \]
if (thid == 0) { temp[n - 1] = 0; } // clear the last element
for (int d = 1; d < n; d *= 2) // traverse down tree & build scan
{
    offset /= 2;
    __syncthreads();
    if (thid < d)
    {
        int ai = offset*(2*thid+1)-1;
        int bi = offset*(2*thid+2)-1;
        float t = temp[ai];
        temp[ai] = temp[bi];
        temp[bi] += t;
    }
    __syncthreads();
    g_odata[2*thid] = temp[2*thid]; // write results to device memory
    g_odata[2*thid+1] = temp[2*thid+1];
}

for $d := \log_2 n$ down to 0 do
    for $k$ from 0 to $n-1$ by $2^{d+1}$ in parallel do
        $t := x[k + 2^d - 1]$
        $x[k + 2^d - 1] := x[k + 2^{d+1} - 1]$
        $x[k + 2^{d+1} - 1] := t + x[k + 2^{d+1} - 1]$
Analysis

```c
__global__ void prescan(float *g_odata, float *g_idata, int n) {
    extern __shared__ float temp[]; // points to shared memory
    int thid = threadIdx.x;
    int offset = 1;
    temp[2*thid] = g_idata[2*thid]; // load input into shared memory
    ...
```

Restriction: Limited to a single thread block
- threadIdx.x is an identifier inside the thread block
- Shared memory is defined in the scope of a thread block only

We need to find a solution that supports arrays of arbitrary size.
Scan - arbitrary array size

1. Divide the large array into blocks that each can be scanned by a single thread block
2. Scan the blocks, and write the total sum of each block to another array of block sums
3. Scan the block sums, generating an array of block increments that are added to all elements in their respective blocks
Scan - arbitrary array size

0. Array of arbitrary values

1. Scan block 0, Scan block 1, Scan block 2, Scan block 3
   - $\Sigma_0$, $\Sigma_1$, $\Sigma_2$, $\Sigma_3$

2. Store block sum to auxiliary array:
   - $\Sigma_0 \Sigma_1 \Sigma_2 \Sigma_3$

3. Scan block sums (recursively):
   - $\Sigma_0 \Sigma_1 \Sigma_2 \Sigma_3$ → scan $\sigma_0 \sigma_1 \sigma_2 \sigma_3$

4. Add $\sigma_0$ to all, Add $\sigma_1$ to all, Add $\sigma_2$ to all, Add $\sigma_3$ to all
   - Final array of scanned values
Performance

Table 2: Performance of the work-efficient, bank conflict free Scan implemented in CUDA compared to a sequential scan implemented in C++. The CUDA scan was executed on an NVIDIA GeForce 8800 GTX GPU, the sequential scan on a single core of an Intel Core Duo Extreme 2.93 GHz.

Table source: Parallel Prefix Sum (Scan) with CUDA (2007), Mark Harris.
References

- Parallel Prefix Sum (Scan) with CUDA (2007), Mark Harris.
- Parallel Prefix Sum (Scan) with CUDA, GPU Gems 3 Chapter 39.